REMARKS

Summary of the Final Office Action

In the Final Office Action, Claims 1-9, 11 and 19-24 were rejected due to purported informalities therein and over the art of record. By the present Amendment and Remarks, Applicant submits that the rejections have been overcome, and respectfully requests reconsideration of the outstanding Office Action and allowance of the present application.

Telephone Interview with Examiner Lewis

Applicant gratefully acknowledges the courtesy extended to their representative by Examiner Lewis in conducting a telephone interview on June 30th, 2004. In the interview, Applicant's representative and Examiner Lewis discussed the outstanding rejections under 35 U.S.C §§ 112 and 103. The Applicant's representative proposed to delete the phrase "the first semiconductor die and the leads being oriented relative to each other" from independent Claims 1 and 19 in an effort to expedite prosecution. The Examiner agreed to withdraw the aforementioned § 112 rejection if an After Final Amendment was submitted reflecting such changes to Claims 1 and 19. On the merits, Applicant's representative respectfully submitted to the Examiner that the outstanding § 103(a) rejection was inappropriate, and therefore should be withdrawn. The Examiner agreed to give further consideration to the Applicant's arguments when presented in an After Final Response.

Traversal of Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 1-9, 11 and 19-24 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the Examiner contends that it is not clear as to what the phrase "oriented relative to each other" means in Claims 1 and 19.

In an effort to expedite prosecution, Applicant has deleted the phrase "the first semiconductor die and the leads being oriented relative to each other" from independent Claims 1 and 19.

In view of the foregoing, Applicant submits that Claims 1-9, 11 and 19-24 are clear and definite, and therefore, comply with 35 U.S.C. § 112, second paragraph. Thus, Applicant respectfully requests that the Examiner reconsider and withdraw the rejections of Claims 1-9, 11 and 19-24 under 35 U.S.C. § 112, second paragraph.

Traversal of Rejection Under 35 U.S.C. § 103(a)

HUANG in view of ABE

Applicant traverses the rejection of Claims 1-6, 9, 11 and 19-24 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,198,171 to Huang et al. [hereinafter "HUANG"] in view of U.S. Patent No. 6,410,979 to Abe [hereinafter "ABE"].

In regard to independent Claims 1 and 19, the Examiner admits that HUANG fails to disclose "portions of the first surface directly attached to the second surface of each of the leads". The Examiner then submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing costs. Further, the Examiner submits that HUANG and ABE are both from the same field of endeavor, and that the purpose disclosed by ABE would have been recognized in the pertinent art of HUANG.

Applicant respectfully disagrees with the Examiner's position.

A Review of HUANG

In the embodiment of the semiconductor package shown in Figure 7 of HUANG, a first or lower chip 304 is shown as being mounted to the top surface of the die pad 318 via a layer of adhesive 322. Disposed about the periphery of the die pad 318 are a plurality of leads 326, each of which includes a first or top surface 328a, and a second or bottom surface 328b which has a stepped structure defining a protruded zone 330. Stacked upon the lower first chip 304 is an upper second chip 310 which is

secured to the first chip 304 by a layer of adhesive 324. As clearly shown in Figure 7, no portion of the lower surface of the chip 304 is attached to the first or top surfaces 328a of the leads 326. Rather, the leads 326 are disposed well outward and outboard of the peripheral edges of the first and second chips 304, 310.

A Review of ABE

ABE discloses a semiconductor device 1 having a leadframe 10 and a semiconductor element 14 which is mounted to the leadframe 10 through the use of an adhesive tape 12. The semiconductor element 14 is electrically connected to the leadframe 10 through the use of bonding wires 16 which, along with the semiconductor element 14, are sealed or encapsulated with a resin material 18. The leadframe 10 of the semiconductor device 1 in the ABE reference includes a plurality of terminal portions 10a which protrude through the substrate mount surface of the resin material 18 and each have a solder layer 19 applied thereto. As is specifically stated in the specification of ABE, the application of the solder layer 19 to each of the terminal portions 10a is made possible by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 which allows the terminal portions 10a to be used as connecting terminals, thereby eliminating the need for solder balls for mounting as required in conventional ball-grid array semiconductor devices, and thus, providing substantially reduced material and manufacturing costs (see ABE specification, column 3, lines 46-58).

In re Claims Independent Claims 1 and 19

Independent Claim 1 as amended recites, *inter alia*, *". . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads . . . ".*

Independent Claim 19 as amended recites, *inter alia*, *". . . the first semiconductor die being directly attached to each of the leads such that each of the*

bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads . . . ".

Applicant respectfully submits that the combined teachings of HUANG and ABE clearly do not teach or suggest any embodiment of a semiconductor package having the aforementioned features as recited in independent Claims 1 and 19.

The manner in which the Examiner modifies HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose

Applicant submits that the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose. Applicant reminds the Examiner that a proposed modification cannot destroy a reference by rendering the prior art invention being modified unsatisfactory for its intended purpose. *In re Gordon*, 733 F.2d 900, 90, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

As discussed above, the Examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE.

A review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304 or repositioned further inboard beneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326. Therefore, the manner in which the Examiner has modified HUANG in view of ABE renders the HUANG reference unsatisfactory for its intended purpose. Furthermore, neither HUANG or ABE, when considered individually or in combination teach or even remotely suggest the spatial relationship between the bond pads 113 (i.e., the bonding pads 308 being oriented between

respective pairs of the leads 326) and leads 130 of the present invention as recited in independent Claims 1 and 19.

Accordingly, it is submitted that the Examiner has inappropriately modified HUANG in view of ABE, and as result destroyed the function of the HUANG reference. Thus, Applicant respectfully submits that the rejection of at least independent Claims 1 and 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Furthermore, the motivation to modify HAUNG with the teachings of ABE as proposed by the Examiner is defective

The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of HUANG to include portions of the die attached to the leads as disclosed in ABE because it aids in reducing manufacturing cost.

The Examiner is first reminded that it must be shown that there was a suggestion, i.e., a motivation to combine something to suggest the desirability, and thus the obviousness, of making the combination. *Lindermann Maschinenhfabrik GMBH v. American Hoist and Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed Cir. 1984). Obviousness cannot be established by combining references without also providing evidence of the motivating force which would impel one skilled in the art to do what the Applicant has done. *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd Pat. App. & Inter. 1993).

To find motivation, the Examiner makes reference to the passage of the specification of ABE beginning in column 1, line 50 and ending in column 2, line 19. However, this language simply mirrors that described above in column 3, lines 46-58 of the ABE reference. In this regard, both the language of this passage and that cited by the Examiner demonstrates that the reduction in manufacturing costs discussed in ABE has absolutely nothing to do with the attachment of the semiconductor element 14 to the leadframe 10 through the use of the adhesive tape 12. Rather, the manufacturing cost reductions discussed in ABE are achieved by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 and

application of the solder layers 19 thereto which allows the terminal portions 10a to be used as connecting terminals. There is simply no teaching or suggestion in the ABE reference regarding a correlation between the reduction in manufacturing costs as argued by the Examiner and the attachment of the semiconductor element 14 to the leadframe 10. Thus, it appears the motivation given by the Examiner to combine the ABE leads to the HUANG package to reduce manufacturing costs is defective.

Accordingly it is submitted that the Examiner has failed to provide sufficient motivation for the proposed modification, and thus the rejection of at least independent Claims 1 and 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn for this additional reason.

Additionally, the Applicant's disclosure may not be used as a template for a rejection (i.e. the Examiner has used impermissible hindsight to find motivation).

Applicant also notes that the Examiner has the initial duty of supplying the factual basis for the rejection and may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis. See *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 177 (CCPA 1967). As stated in *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1533, 220 USPQ 303, 312-313 (Fed. Cir. 1983), cert denied, 469 U.S. 851 (1984):

> [t]o imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which the inventor taught is used against it teacher.

Applicant submits that it is highly likely that the modification of HUANG in view of ABE as proposed by the Examiner has resulted from a review of Applicant's disclosure and the application of impermissible hindsight to find motivation.

In particular, Applicant submits that the Examiner has merely used the Applicant's disclosure as a template to find obvious the features of independent Claim 1 which recites, *inter alia*, *". . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads such that each of the*

bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads . . . ".

Moreover, Applicant submits that the Examiner has merely used the Applicant's disclosure as a template to find obvious the features of independent Claim 19 as amended which recites, *inter alia*, *". . . the first semiconductor die being directly attached to each of the leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads . . . ".*

Accordingly, it is submitted that the Examiner has used impermissible hindsight to find motivation for the proposed modification, and thus the rejection of at least independent Claims 1 and 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn for this additional reason.

Moreover, the combination which the Examiner presents does not result in the invention that the Applicant claims, therefore, the aforementioned rejection is inappropriate.

With respect to the aforementioned rejection, the Examiner has not provided a prior art reference or references which teach or suggest ***all*** the claim limitations of the pending claims.

To establish a prima facie case of obviousness, *the prior art reference (or references when combined) must teach or suggest **all** the claim limitations.* See *Litton Industrial Products, Inc. v. Solid State Systems, Corp.*, 755 F.2d 158, 164, 225 U.S.P.Q. 34, 38 (Fed. Cir. 1985) ("The references fail not only to expressly disclose the claimed invention as a whole, but also to suggest to one of ordinary skill in the art modifications needed to meet ***all*** the claim limitations").

Even assuming, *arguendo*, that the hypothetical combination of the HUANG and ABE references is proper (which the Applicant disputes), Applicant respectfully submits that such combination still does not teach or suggest the relative orientations

between the bond pads of the first semiconductor die and the leads as recited in independent Claims 1 and 19.

As already discussed, a review of Figure 4 of HUANG and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304 or positioned further inboard underneath first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326.

On the other hand, the present invention clearly teaches and claims a spatial relationship between the bond pads 113 and leads 130. In this regard, there is clearly no teaching in HUANG regarding the orientation of the first bonding pads 308 of the first chip 304 between respective pairs of the leads 326.

In particular, neither HUANG nor ABE, when considered individually or in combination teach or suggest, *inter alia*, *". . . portions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads* ***such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads*** *. . . "* as is recited in independent Claim 1.

Furthermore, neither HUANG nor ABE, when considered individually or in combination teach or suggest, *inter alia, ". . . the first semiconductor die being directly attached to each of the* ***leads such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads*** *. . . "* as is recited in independent Claim 19.

Accordingly, Applicant submits that no proper combination of HUANG and ABE discloses or suggests at least the above-noted features of the present invention, and thus the rejection of at least independent Claims 1 and 19 under 35 U.S.C. § 103(a) is improper and should be withdrawn for this additional reason.

In re Claims Dependent Claims 2-6, 9, 11 and 20-24

Furthermore, Applicant submits that dependent Claims 2-6, 9, 11 and 20-24 are allowable for the reason that these claims depend from allowable independent Claims 1 and 19 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejections of dependent Claims 2-6, 9, 11 and 20-24 under 35 U.S.C. § 103(a) and indicate that these Claims are allowable.

HUANG in view of ABE and SONG

Applicant traverses the rejection of Claims 7 and 8 under 35 U.S.C. § 103(a) as being obvious over HUANG in view ABE and Korean Publication No. 2002049944 to Song [hereinafter "SONG"].

In regard to dependent Claim 7, the Examiner admits that HUANG fails to disclose "the bottom surface of the die paddle [being] exposed". The Examiner then submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of HUANG to include a die paddle that has a bottom surface that is exposed as disclosed in SONG because it aids in providing a simplified fabricating process. Further, the Examiner submits that since HUANG and SONG are both from the same field of endeavor, the purpose disclosed by SONG would have been recognized in the pertinent art of HUANG.

For the reasons discussed above, Applicant submits that independent Claims 1 and 19 are allowable. Furthermore, Applicant submits that dependent Claims 7 and 8 are allowable at least for the reason that these claims depend from allowable independent Claims 1 and 19 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejections of Claims 7 and 8 under 35 U.S.C. § 103(a) and indicate that these claims are allowable.

Application is Allowable

Applicant respectfully submits that each and every pending claim of the present application meets the requirements for patentability, and respectfully requests the Examiner to indicate the allowance of such claims.

CONCLUSION

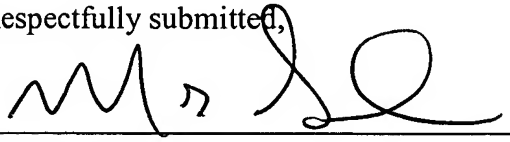
In view of the foregoing, it is submitted that none of the references of record, when considered either alone or in any proper combination thereof, anticipate or render obvious the Applicant's invention as recited in Claims 1-9, 11 and 19-24. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Applicant respectfully submits that each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. §§ 112, 102 and 103. Accordingly, allowance of the present application and all the claims therein is respectfully requested and believed to be appropriate.

Further, any amendments to the claims which have been made in this response and which have not been noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

Date: 3/3/04 By: 

Mark B. Garred
Reg. No. 34,823
STETINA BRUNDA GARRED & BRUCKER
75 Enterprise, Suite 250
Aliso Viejo, CA 92656
(949) 855-1246

Customer No. 007663